WHAT IS CLAIMED IS:

1. A method for loading pixels into a temporary memory, comprising:

loading a block of pixels into said temporary memory;

loading a staging memory with pixels for updating said block of pixels, by rearranging said pixels so that an update group of pixels can be accessed in parallel from said staging memory;

updating said block of pixels in said temporary memory with an update group of pixels from said staging memory in parallel.

2. The method of claim 1 wherein said temporary memory is connected to a processing unit for comparing said block of pixels to a second block of pixels.

3. The method of claim 2 wherein said temporary memory is a two-dimensional shift register, and wherein said update group of pixels corresponds to a shifted row or column of said block of data.

4. The method of claim 2 wherein said processing unit performs a comparison for a motion estimation algorithm.

5. The method of claim 1 wherein said staging memory comprises banks of memories, each bank providing a different one of said update group of pixels.

6. The method of claim 5 wherein said update group of pixels is a row or column.

7. The method of claim 1 further comprising providing a search pattern that can be executed by loading said temporary memory, in a single cycle, with pixels to provide a next block to be searched.

8. The method of claim 7 wherein said search pattern is a spiral search pattern.

9. The method of claim 1 wherein said rearranging of said pixels comprises reordering said pixels in each row so that each pixels from a single column are spread across a plurality of columns so that they can be accessed in parallel.

10. A method for loading pixels into a temporary memory, comprising:

loading a block of pixels into said temporary memory, said temporary memory being a two-dimensional shift register;

loading a plurality of memory banks with pixels for updating said block of pixels in said two-dimensional shift register, by rearranging said pixels so that a column or row of pixels can be accessed in parallel from said memory banks;

executing a search pattern wherein each block in said search pattern differs from a previous block by a single row or column; and

updating said block of pixels in said temporary memory with a new row or column from said memory banks in parallel.

11. The method of claim 10 wherein said search pattern is a spiral search pattern.

12. An apparatus for loading pixels into a temporary memory, comprising:

a temporary memory for storing a block of pixels;

a staging memory for storing new pixels for updating said block of pixels;

an address translator for rearranging said new pixels so that an update group of said new pixels can be accessed in parallel from said staging memory;

an addressing unit for providing a block of pixels in parallel from said staging memory to said temporary memory.

13. The apparatus of claim 12 wherein said addressing unit reorders pixels from said staging memory.

14. The apparatus of claim 12 wherein said staging memory comprises a plurality of memory banks.

15. The apparatus of claim 12 wherein said staging memory comprises SRAM memory.

16. The apparatus of claim 12 wherein said temporary memory is a two-dimensional shift register, and wherein said update group of pixels corresponds to a shifted row or column of said block of data.

17. The apparatus of claim 12 wherein said temporary memory is connected to a processing unit for comparing said block of pixels to a second block of pixels.

18. The apparatus of claim 17 wherein said processing unit performs a comparison for a motion estimation algorithm.

19. An apparatus, comprising:

a two dimensional shift register for storing a block of pixels;

a processing unit coupled to said two dimensional shift register, said processing unit being configured to simultaneously compare each pixel in said block of pixels with a reference block of pixels;

a plurality of memory banks for storing new pixels for updating said block of pixels;

an address translator coupled to an input to said plurality of memory banks for rearranging said new pixels so that an update group of said new pixels can be accessed in parallel from said plurality of memory banks;

an addressing unit for reordering a group of pixels accessed in parallel from said plurality of memory banks to said two dimensional shift register, correcting for rearrangements made by said address translator to allow said new pixels to be accessed in parallel.

20. The apparatus of claim 19 further comprising:

four buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom.